UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE DEPARTMENT OF ELECTRONIC ENGINEERING

SUPPLEMENTARY MAIN EXAMINATION 2005

Title of the Paper: **ELECTRONICS II**

Course Number: E440 PAPER 2, Practical Examination

Time Allowed: Three Hours.

Instructions:

Points for different sections are shown in the right hand margin.

Special Requirement:

One floppy disc (labeled with your I.D. and name), which must be handed in, together with your answer sheet, at the end of the examination

THIS PAPER HAS 2 PAGES, INCLUDING THIS PAGE

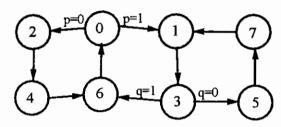
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A 3-Mode Sequencer

System Description:

This sequencer has 3 modes of operation, selectable through the external input p and q parameters. The description of its operation is given below by the state diagram. Do the design, implement, and simulation.

State Diagram:



Design Details:

Implementation may be in the form of a ROM, a PLA, or traditional logic gates (simpler). If a ROM or a PLA, a table of the address and its content is required instead of flip-flop functions. Give the following items:

State table

Flip-flop input functions

(each K-map-5pts, subtotal-15, functions-10pts)

Sequencer circuit diagram: this will be the one shown in the simulation file

25pts

Simulation:

30pts

parts of the simulation test:

parts of the simulation test.	
a. the choice of the components.	6pts
b. set of proper monitor points in the circuit.	6pts
c. wiring scheme.	10pts
d. proper remarks or notes on the circuit diagram.	8pts