UNIVERSITY OF SWAZILAND
FACULTY OF SCIENCE

DEPARTMENT OF ELECTRONIC ENGINEERING
MAIN EXAMINATION, DECEMBER 2007

TITLE OF PAPER : ANALOGUE ELECTRONICS

COURSE NUMBER : E361

TIME ALLOWED : THREE HOURS

INSTRUCTIONS : READ EACH QUESTION CAREFULLY ANSWER ANY **FOUR** OUT OF **FIVE** QUESTIONS. EACH QUESTION CARRIES **25 MARKS**. MARKS FOR EACH SECTION ARE SHOWN ON THE RIGHT-HAND MARGIN.

THIS PAPER HAS 6 PAGES INCLUDING THIS PAGE.

THIS PAPER IS NOT TO BE OPENED UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

QUESTION 1

Calculate the values of R_1, R_2, R_3 and R_4 for a common emitter transistor stage of Figure 1, with the following bias parameters :

V_{BEQ} = 0.7 V, V_{CEQ} = 8.2 V, I_{CQ} = 1mA.

The total input resistance of the circuit is 3.6 kΩ, the voltage gain = -300 and β = 240.

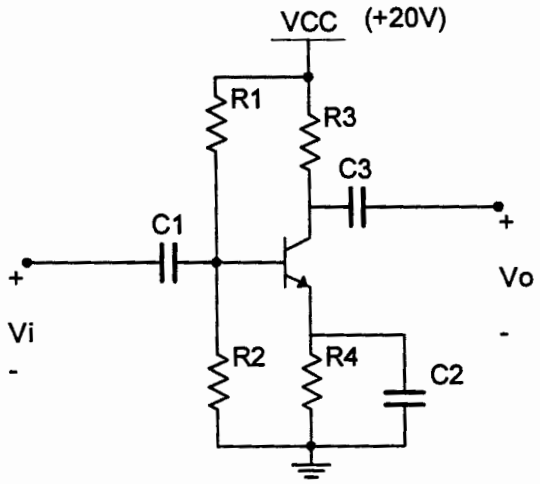


Figure 1

(25 marks)

QUESTION 2

(a) The silicon diodes used in Figure 2 have $R_f = 40\ \Omega$, $V_\gamma = 0.7$ V, $I_s = 0$ and $R_r = \infty$.

(i) Compute the output voltage , V_o.

(12 marks)

(ii) Hence, obtain the voltage across the diode D_1 .

(3 marks)

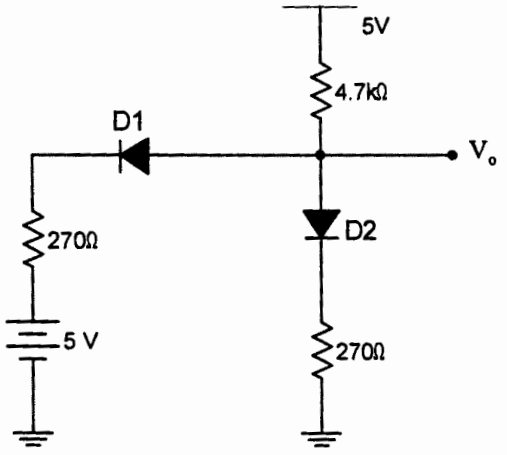


Figure 2

(b) The input voltage *vi* in Figure 3 varies from 0.3 V to 0.7 V. Vcc = 10 V.

(i) Explain how variation of the input voltage V_s will affect the operating modes of the transistor.

(7 marks)

(ii) Plot V_o *as* V_s varies from 0.3 V to 0.7 V.

(3 marks)

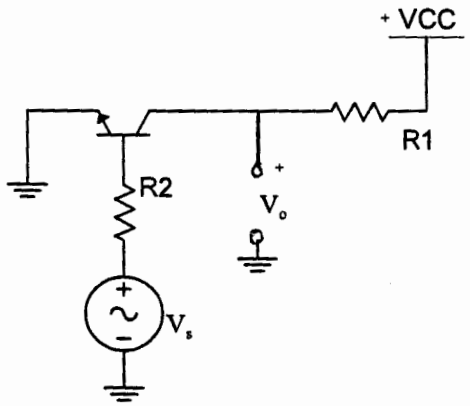


Figure 3

QUESTION 3

(a) The operational amplifier may be used to perform a wide variety of functions, one of which is as depicted in Figure 4. The input voltages are V_1, V_2, V_3 and the output is V_0.

(i) List four characteristics of an ideal op amp. (4 marks)

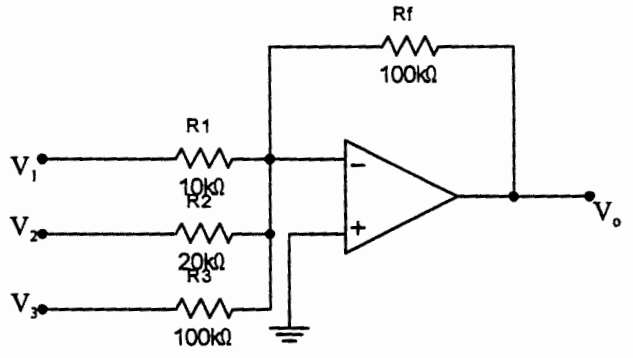


Figure 4

(ii) Derive an expression for the output voltage in terms of the three input voltages. (6 marks)

(iii) Determine the gain factors for the three input signals. (6 marks)

(iv) Hence, obtain the output voltage for the following input conditions: $V_1 = 0.5$ V, $V_2 = 0.8$ V, $V_3 = -3$ V. (3 marks)

(b) The three input resistors of Figure 4 are removed and replaced by a 1 μf capacitor. Identify the function of this circuit by deriving an expression for the output voltage in terms of the input voltage.

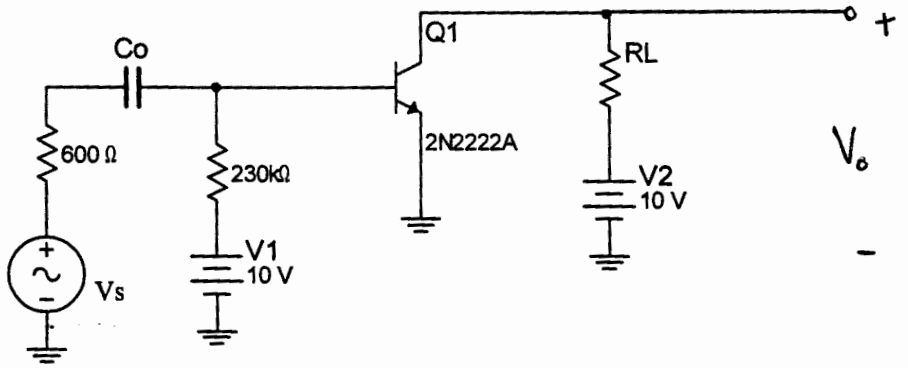
(6 marks)

QUESTION 4

The transistor of Figure 5, is biased in the forward active region at an operating point of $I_B = 50\ \mu A$ and $V_{CE} = 5$ V. It has $\beta = 200$, a base spreading resistance $r_b = 100\ \Omega$ and the output resistance $r_o = 100\ k\Omega$.

(i) What is the function of capacitor C_0? (2 marks)

(ii) Present the low-frequency small - signal hybrid - π equivalent circuit of Figure 5. (4 marks)



Figurer 5

(b) Assuming operation at room temperature, compute the

(i) output resistance R_o , and (8 marks)
(ii) the voltage gain, v_o/v_s (11 marks)

Derive any formula used.

QUESTION 5

An n - channel enhancement MOSFET is connected as shown in Figure 6. The quiescent drain current I_{DS} = 190 μA, gm = 0.123 mA/V and r_{ds} = 40 Ω. The 0.12 V variation in the gate - source bias is due to a 0.3 V variation in V_{DD}

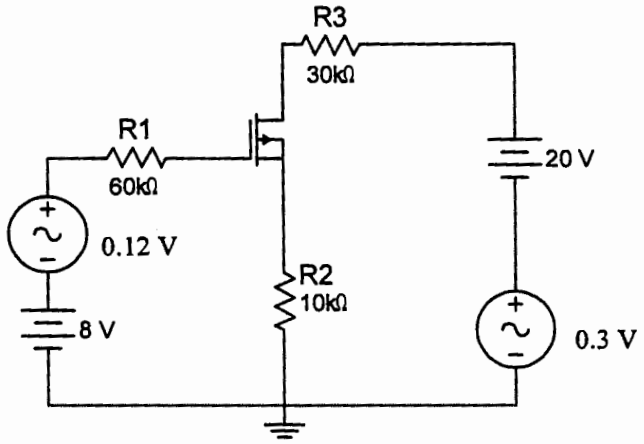


Figure 6

(i) Construct the small - signal model of the circuit in Figure 6.

(4 marks)

(ii) Compute the total voltage v_{DS} and the total current i_{DS}.

(18 marks)

(iii) What percentage change occurred in v_{DS} as a result of the variation in V_{DD}? Can this small change be resolved by use of the bias line method? Explain.

(3 marks)