UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
DEPARTMENT OF ELECTRONIC ENGINEERING

MAIN EXAMINATION, MAY 2008

Title of the Paper:	**DIGITAL ELECTRONICS I**
Course Number:	**E362**
Time Allowed:	**Three Hours.**

Instructions:

1. Answer any FIVE (5) of the six questions.
2. Each question carries 20 marks, distributed as shown next to the right hand margin

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QUESTION 1

a) Using the tabulation method, simplify the following Boolean function F:
F(v, w, x, y, z)=Σ(0, 2, 4, 6, 10, 11, 12, 14, 15, 16)
(hex numbers in the brackets of the above function) [10]

b) Implement the Boolean function below using only NAND gates. Assume that complement inputs are available only at the input terminals and nowhere else. The implementation must have its function support.
$F(A,B,C,D,E) = (\overline{A}+B)(C\overline{D}+\overline{E})$ [10]

QUESTION 2

a) Using a minimum number of NOR gates only, implement the circuits for the expressions below. Assume that both normal and complement inputs are available.

(i) $F_1 = A \oplus B \oplus C$ [5]

(ii) $F_2 = (A + BC)(A + B + CD + \overline{A}C)$ [5]

b) Using the block diagram transformation method, implement the function below with NOR gates only. The circuit diagram should be multi-level. Assume that both normal and complement inputs are available, and show all necessary working.

$F = C(B + AD) + A(\overline{B} + C\overline{D})$ [10]

QUESTION 3

a) (i) Implement the sum S of a Binary Full Adder with AND, OR and NOT gates. [5]

(ii) Verify that the sum S for a full adder can be put in the form $S = A \oplus B \oplus C_{in}$, and implement this form in gates. [10]

b) Implement the function F with an 8-to-1 Multiplexer. You may make x, y and z selectors.

$$F = \bar{w}\bar{x}\bar{y}\bar{z} + \bar{w}x\bar{y}z + \bar{w}xy\bar{z} + \bar{w}xyz + w\bar{x}\bar{y}\bar{z} + w\bar{x}\bar{y}z + wx\bar{y}\bar{z} + wxy\bar{z}$$

[5]

QUESTION 4

a) Using a three-bit message code, show how an even-parity generator can be implemented using gates. ***(The final circuit implementation must be in XOR and/or XNOR gates. Show all necessary working)*** [6]

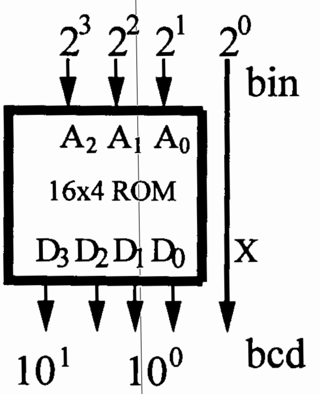
b) Do a parity check on the message generated by the even parity generator in (a), and show that the expression for the even parity checker function, C, can be written in XOR/XNOR operations only. [7]

c) Create a 4-bit reflected (Gray) code from the start byte, 1001. [7]

QUESTION 5

a) Three 4-to-1 Multiplexers are available. Arrange the three Multiplexers into a larger Multiplexer with the largest number of inputs possible and least number of address-bits (*variables of the selector lines*). How many address bits and how many inputs are in your solution? Show a clearly labeled diagram and list the address of each input. [10]

b) The 16x4 ROM together with the 2^0 line as shown in the figure below is to be used to convert a 4-bit binary number to its corresponding 2-digit BCD number. Specify the truth table for the ROM. (Hint: binary1111 converts to BCD 1, 0101=$15_{dec.}$). [10]



QUESTION 6

Design a PLA that implements the following set of logic functions:

$$X = a\,b\,c + a\,\overline{b}\,c + \overline{a}\,b\,c + \overline{a}\,\overline{b}\,\overline{c}$$

$$Y = a\,b\,\overline{c} + a\,\overline{b}\,c + \overline{a}\,\overline{b}\,c$$

$$Z = a\,b\,\overline{c} + \overline{a}\,b\,\overline{c} + \overline{a}\,\overline{b}\,\overline{c}$$

[20]