

UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE

DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING

DIGITAL SYSTEMS I

COURSE CODE – EE322

MAIN EXAMINATION DECEMBER 2011

DURATION OF THE EXAMINATION - 3 HOURS

INSTRUCTIONS TO CANDIDATES

- i. There are FIVE questions in this paper. Answer any FOUR questions only.
- ii. Each question carries equal marks.
- iii. Show all your steps clearly in any calculations.
- iv. State clearly any assumptions made.
- v. Start each new question on a fresh page.

DO NOT OPEN THIS PAPER UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Question 1

(a) Using the tabular method, minimize the following Boolean function:

$$F(A, B, C, D) = \sum(0, 2, 3, 5, 7, 8, 10, 11, 14, 15) \quad [10]$$

(b) Simplify the following using a k-map:

(i) $F = C'D + ABC' + ABD' + A'B'D$ [7]

(ii) $F(A, B, C, D) = \sum(0, 6, 8, 13, 14)$ [4]
 $d(A, B, C, D) = \sum(2, 4, 10)$

(c) Using Boolean algebra simplify the following Boolean expression to a minimum number of literals:

$$F = wx' + y'z' + w'yz' \quad [4]$$

Question 2

Analyse the combinational circuit shown in Figure Q2 and determine its truth table. Show all working.

[25]

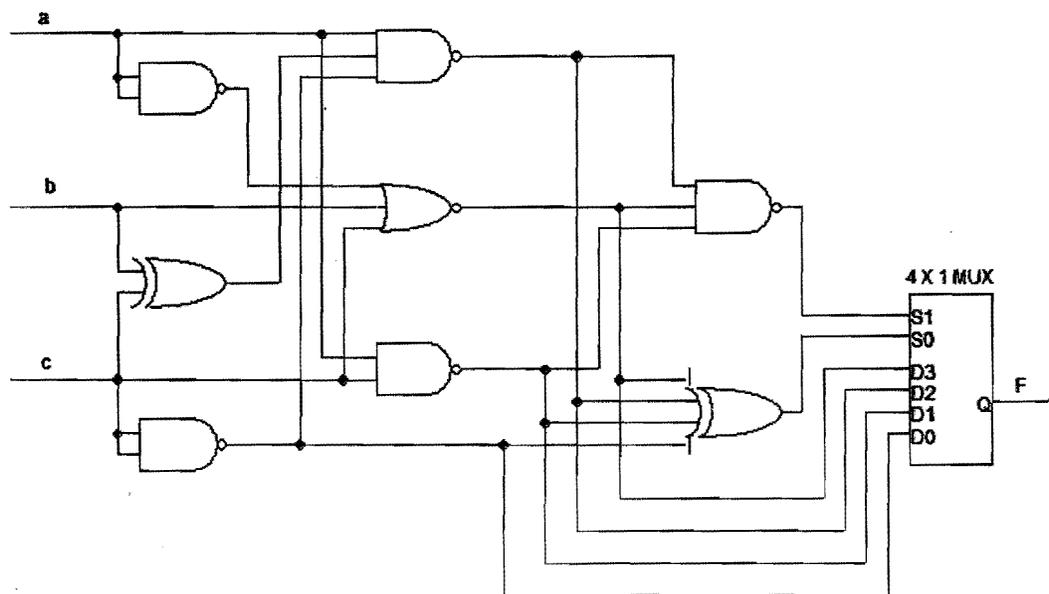


Figure Q2: Diagram for question 2

Question 3

a) Derive the Boolean expressions for the output sum and output carry in a full adder circuit with inputs x_i , y_i , and c_i .

[6]

- b) Assuming that the *carry propagate* and *carry generate* are defined as

$$P_i = x_i + y_i$$

$$G_i = x_i y_i$$

respectively, show that the output carry and output sum of a full adder becomes

$$C_{i+1} = (C_i G_i + P_i) \quad [8]$$

$$S_i = (P_i G_i) \oplus C_i \quad [7]$$

- c) Design a half-subtractor circuit with inputs x and y and outputs D and B . The circuit subtracts the bits $x - y$ and places the difference in D and the borrow in B .

[4]

Question 4

- (a) Figure Q4 is a waveform showing the behavior of a combinational circuit. A , B , and C are inputs, and X and Y are outputs. Implement the circuit and determine the function the circuit performs. [13]

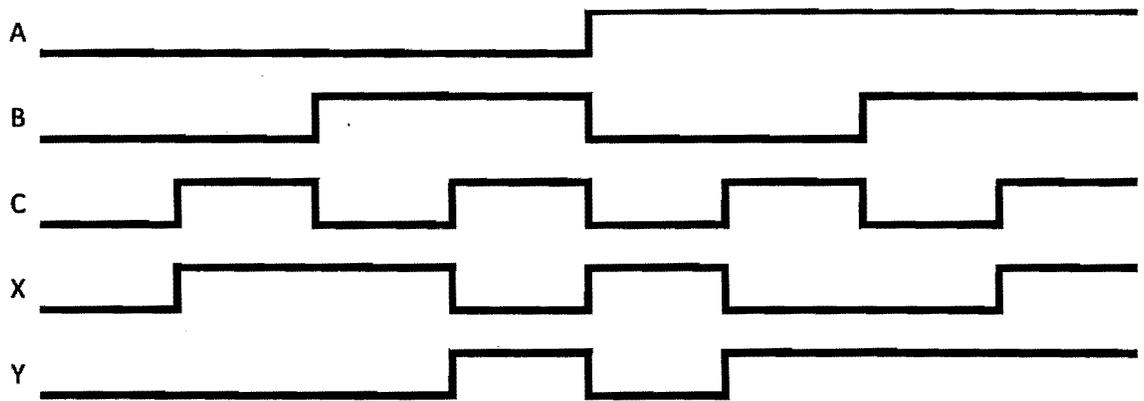


Figure Q4: Diagram for question 4 (a)

- (b) Design a 4-bit Magnitude Comparator which compares two 4-bit binary numbers A , B and determines whether $A < B$, $A > B$, or $A = B$. [12]

Question 5

- a) A combinational circuit is defined by the following three Boolean functions:

$$F_1(A, B, C) = \sum(2, 4, 7)$$

$$F_2(A, B, C) = \sum(0, 3)$$

$$F_3(A, B, C) = \sum(0, 2, 3, 4, 7)$$

Design the circuit with a decoder and a minimum number of external NAND gates. [7]

- b)
- i. Specify the truth table of an hexadecimal-to-binary priority encoder. In your truth table, provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. [8]
 - ii. What will be the value of the four outputs if inputs D9 and D6 are at 1 at the same time? [1]
- c) Implement the following Boolean function with a 4 x 1 multiplexer and external gates. [5]

$$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$$

- d) An 8 x 1 multiplexer has inputs A, B, and C connected to the selection inputs S_2 , S_1 , and S_0 , respectively. The data inputs I_0 through I_7 are as follows: $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$. Determine the Boolean function that the multiplexer implements (express it as sum of products). [4]

END OF PAPER