University of Swaziland
Faculty of Science and Engineering
Department of Electrical and Electronic Engineering

Main Examination 2014

Title of Paper:	Analogue Design I
Course Number:	EE321
Time Allowed:	3 hrs

Instructions:

1. Answer all four (4) questions.
2. Each question carries 25 marks.
3. Where appropriate, $V_{BE} = V_D = 0.7V$, $V_T = 25mV$.
4. E12 range: 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2

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This paper contains nine (7) pages including this page.

Question 1

a) A particular BJT operating at $I_C = 2mA$ has $C_\mu = 1pF$, $C_\pi = 10pF$ and $\beta = 150$. Calculate:

i) f_T [5]

ii) f_β [2]

b) Using an ideal op-amp, design the inverting low-pass amplifier circuit shown in Fig. 1(a) having a pole frequency of $3kHz$. [7]

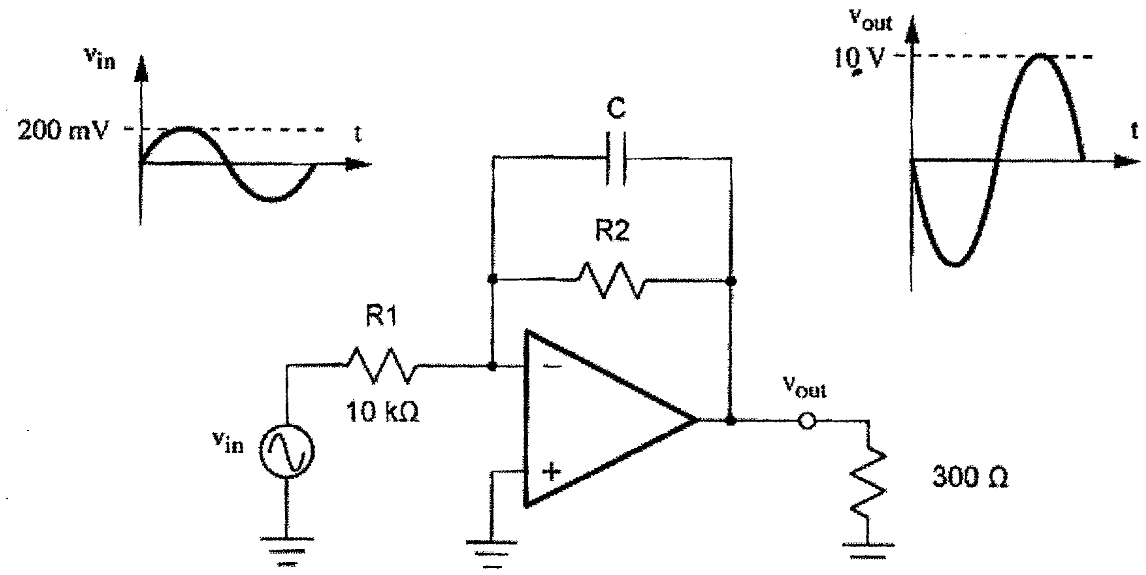

Fig. 1(a)

c) What is the main feature of the differential amplifier? [1]

d) Consider the common base amplifier shown in Fig. 1(b) with $R_L = 10k\Omega$, $R_C = 10k\Omega$, $V_{CC} = 10V$ and $R_{sig} = 100\Omega$. Note $I = I_E$.

i) To what value must I be set in order that the input resistance is 100Ω? [5]

ii) What is the resulting gain from the source to the load? Assume $\alpha = 1$? [5]

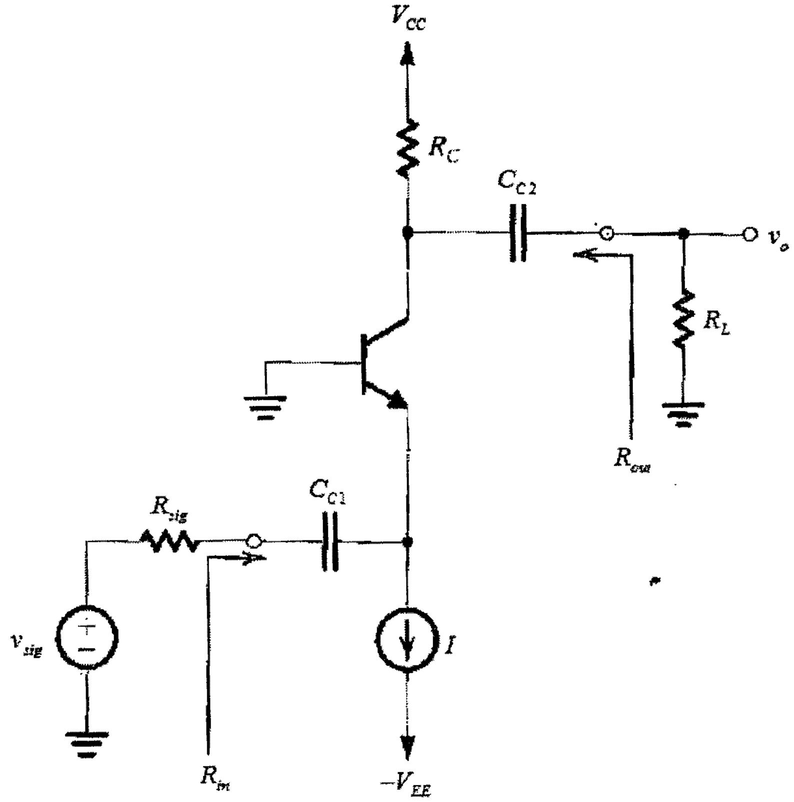

Fig. 1(b)

Question 2

iii) In the circuit shown in Fig. 2(a), v_{sig} is a small sine wave signal with zero average. The transistor β is 100. Note: **Do not make any assumptions in this question.**

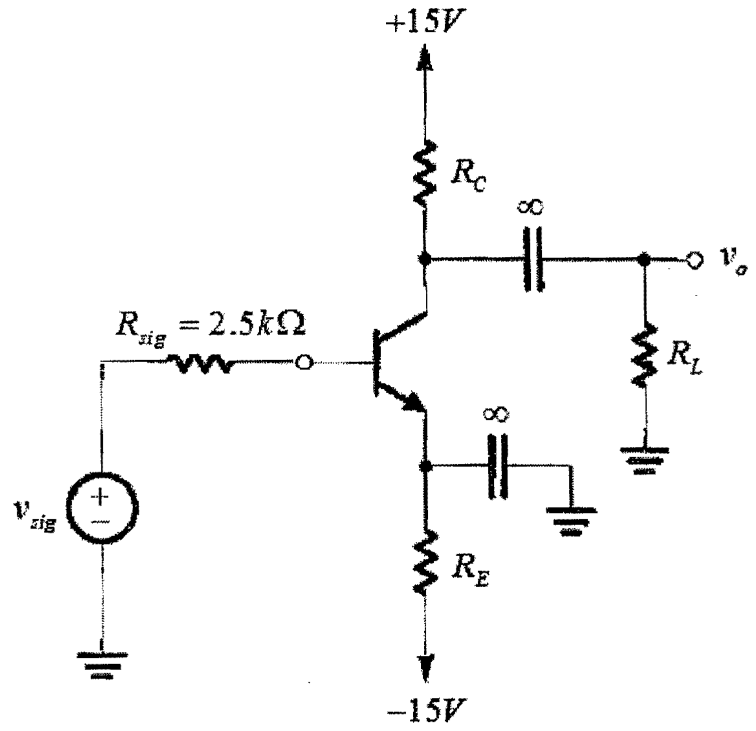

Fig. 2(a)

i) Find the value of R_E to establish a dc emitter current, I_E of about $0.5mA$. [5]

ii) Find R_C to establish a dc collector voltage, V_C of about $5V$. [3]

iii) For $R_L = 10k\Omega$ and the transistor $r_o = 200k\Omega$, draw the small signal equivalent circuit of the amplifier and determine its overall voltage gain, $\dfrac{v_o}{v_{sig}}$. [10]

iv) Differentiate between stagger tuning and synchronous tuning, and for each amplifier sketch the corresponding frequency response. [4]

v) An op-amp has a slew rate of $10V/\mu s$, full-power bandwidth, $\omega_M = 2\times 10^6 rad/\sec$. What is the rated output voltage, $v_{o\max}$? [3]

Question 3

a) Using the topology of Fig. 3(a), design an amplifier to operate between a $10k\Omega$ source and a $2k\Omega$ load with an overall gain of $-8V/V$. The power supply available is $9V$. Use a dc emitter current, I_E of $2mA$ and a current of about one-tenth of that passes through $R1$ and $R2$ in the voltage divider that feeds the base, with the dc voltage, V_{Th} at the base about one-third of the supply. The transistor available has $\beta = 100$ and $V_A = 100V$. **Do not make any assumptions.** Use standard resistor values. [15]

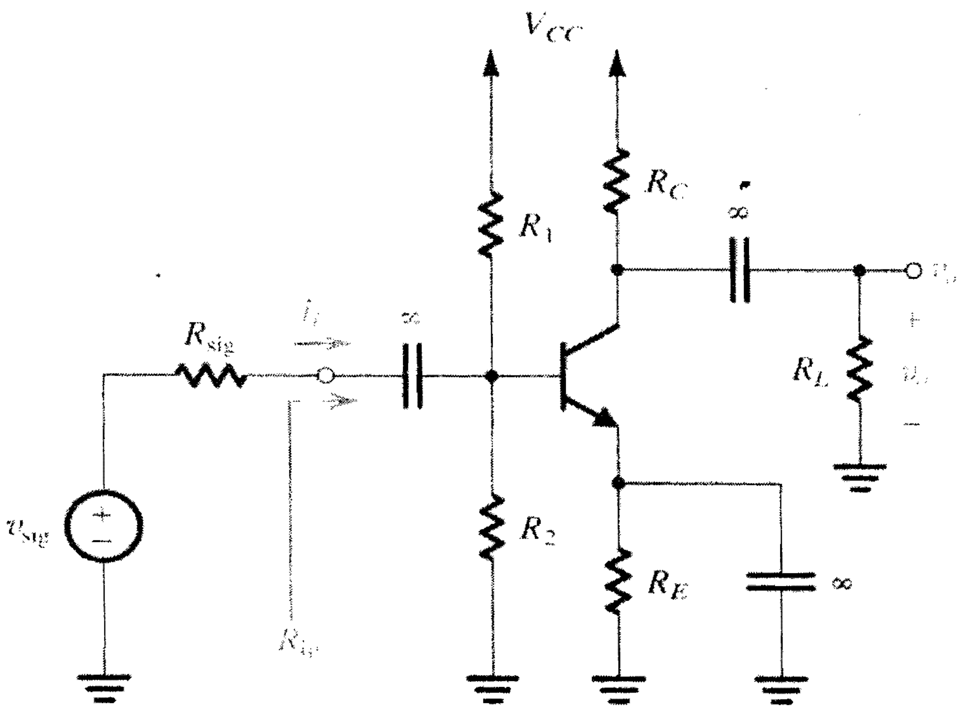

Fig. 3(a)

b) A parallel circuit has a capacitor of $100pF$ in one branch and an inductor of $100\mu H$ plus a resistance of 10Ω in the second branch. The line voltage is $10V$. Find the:

i) Resonant frequency, f_0. [3]

ii) Circuit impedance at resonance, Z_r. [2]

iii) Line current at resonance, I. [2]

c) State 3 advantages of Fixed-Biasing or Base Resistor Biasing [3]

Question 4

a) For the amplifier shown in Fig. 4(a), let $C_{C1} = 1\mu F$.

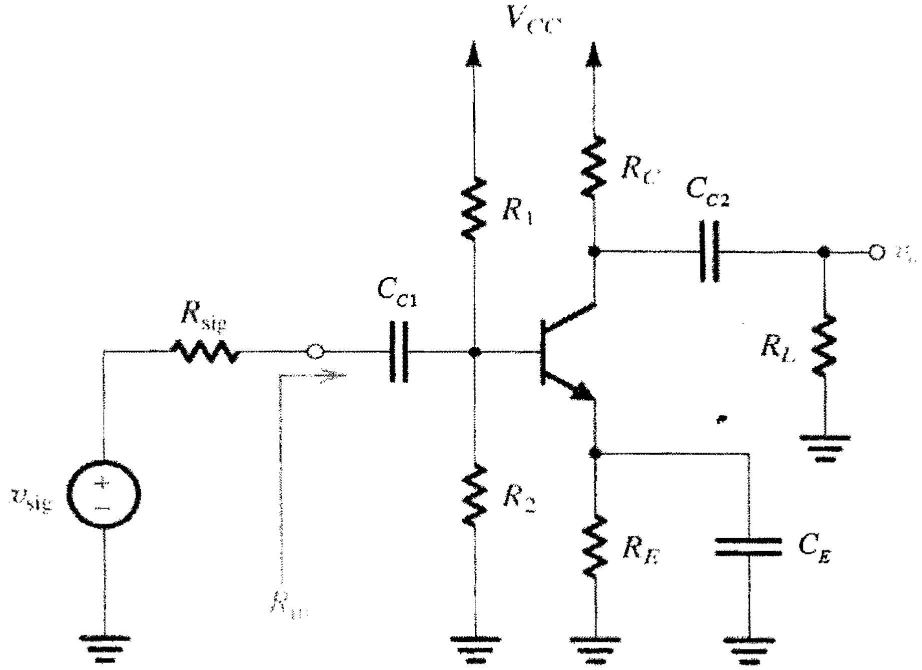

Fig. 4(a)

i) Find the break frequency, f_{p1} resulting from C_{C1}. [5]

ii) Given that $f_{C2} = 15.55Hz$ and $f_{C_E} = 144.95Hz$. Calculate the overall the 3-dB low frequency, f_L of the amplifier. [2]

b) Find an expression for the voltage gain, $\frac{v_{out}}{v_{in}}$ of the circuit in Fig. 4(b). Assume the op-amp is ideal. [4]

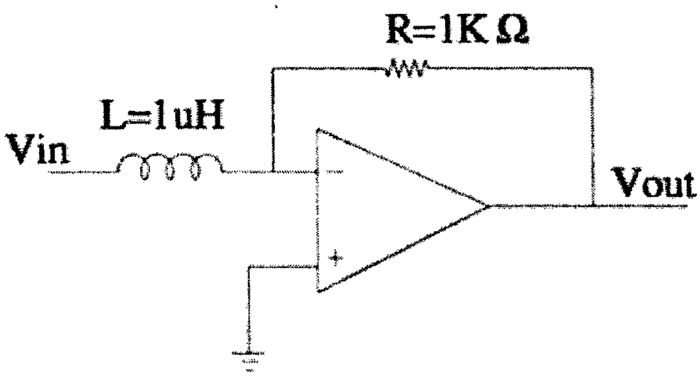

Fig. 4(b)

c) Consider Fig. 4(c), which shows a capacitor between the input and output terminals.

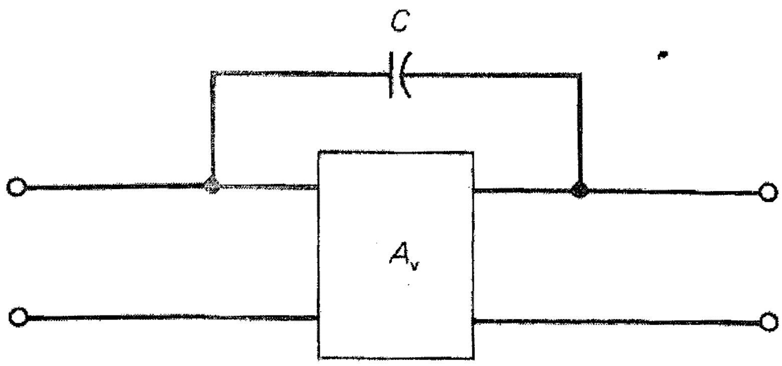

Fig. 4(c)

Using Miller's theorem write equations for the input and output capacitances. [4]

d) The input voltages of an op-amp are $v_2 = 1005\mu V$ and $v_1 = 995\mu V$. The op-amp parameters are $CMRR = 100dB$ and $A_d = 2\times10^5$. Determine the:

i) Differential voltage, v_d. [1]
ii) Common-mode voltage, v_C. [1]
iii) Common-mode gain, A_C. [4]
iv) Output voltage, v_o. [4]