Faculty of Science
Department of Electrical and Electronic Engineering
Main Examination 2014

Title of Paper : **Digital Systems I**

University of Swaziland

Course Number : **EE322**

Time Allowed : **3 hrs**

Instructions :

1. **Answer all four (4) questions**
2. **Each question carries 25 marks**
3. **Useful information is attached at the end of the question paper**

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The paper consists of five (5) pages including the cover page

Question 1 [25]

a) I want to schedule a meeting among 6 individuals, namely Alice, Brian, Charles, David, Elise and Frank. The meeting must be scheduled so that the following rules are satisfied

- ✓ Exactly one of Alice and Brian must be in the meeting
- ✓ Charles and David must be present in the meeting together. If Charles is not available, David and Frank must be in the meeting together. However, all three of Charles, David and Frank must not be present
- ✓ Elise is the manager of the group, so she must be present in the meeting

Each of the 6 team members indicates to me their availability for the meeting. I would like to construct a logic netlist with a single output g, such that g is equals to '1' whenever the meeting can be scheduled

i. List the Boolean variables that you will need for the netlist. [2]
ii. Write down what both values of each variable indicate. [2]
iii. Draw the logic netlist using the gate types we discussed in class. [4]
iv. Write down the netlist as a set of logic equation. [2]

b) Consider the following Boolean function.

$$f = ab'cd' + ab'cd + a'b'cd + a'b'c'd + a'bcd + a'bcd'$$

The don't care points of f are $ab'c'd'$

i. Find the minimum realization of the above function. [7]
ii. Find the minimum NOR-NOR realization of the above function. [8]

Question 2 [25]

a) Suppose I have a 3-input NAND gate. Assume that it is connected in the configurations shown in figure 2.1. What is the logic function of *f* and *g*?[5]

Configuration A Configuration B

Figure 2.1

For the rest of this question, consider the circuit on figure 2.2.

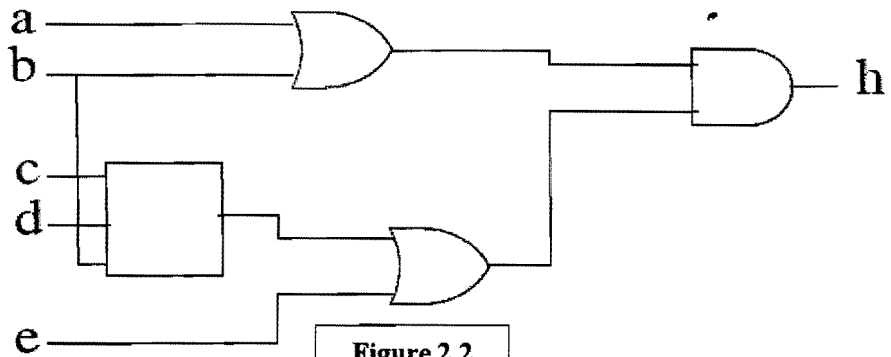

Figure 2.2

b) Change the *box* gate into *bcd +b'c'd'* and redraw the circuit so that it uses OR, AND or NOT gates. [5]

c) Now convert the circuit of the previous part, into another circuit that uses only 3-input NAND gates. [10]

d) Convert the following decimal numbers to the base indicated

i. 7562 to octal [2]
ii. 1938 to hexadecimal [2]
iii. 175 to binary [1]

Question 3 [25]

a) Using 2×4 decoder a one 4×1 multiplexer, design a circuit with the following properties: it has two 2-bit binary number input $(x_1\ x_0)$ $(y_1\ y_0)$ and 2 input, $F_1\ F_0$ to select the function of the circuit:

- EQ outputs a 1 if the two inputs are equal
- GT outputs a 1 if the X is larger than Y
- LTE outputs a 1 if the X is smaller or equal to Y
- NULL outputs a 0

You must use a minimum number of 2×4 decoders with enables (i.e if enable is 0 all outputs are 0, otherwise, the output is 1 for the minterm) and a minimum number of additional gates and only one 4×1 MUX.

Show the circuit diagram with all the **pins to the decoder and multiplexer labelled properly.** States any assumptions you are making in your design. [15]

b) Show the following operations using 2's complement:

i. 10000111 – 1011001 [2]
ii. 1011001 – 1000011 [2]
iii. 0.1001 – 0.0101 [3]
iv. 0.0101 – 0.1001 [3]

Question 4 [25]

a) From the following state diagram, create the state table, and corresponding circuit using D flip-flops. [13]

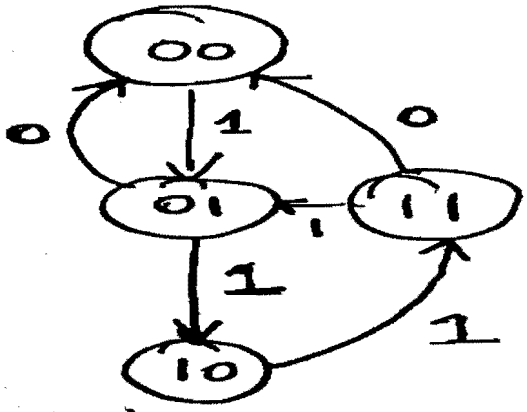

Figure 4.1

b) Derive the state diagram for the following circuit. Transitions should be marked based on both inputs x and y, using the convention xy. Output z should be encoded in the state. [12]

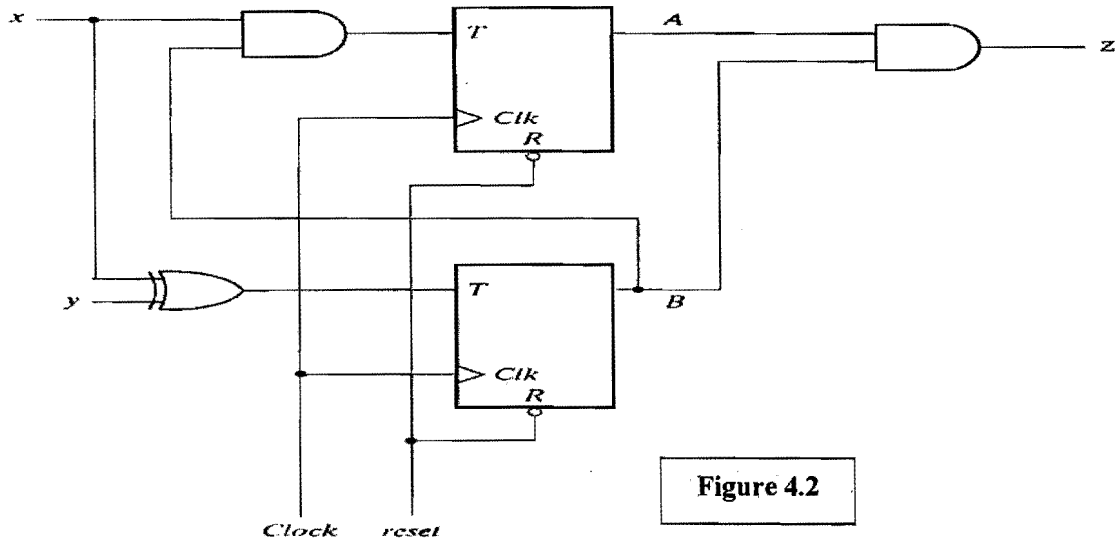

Figure 4.2