UNIVERSITY OF SWAZILAND

MAIN EXAMINATION, SECOND SEMESTER MAY 2015

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: MICROCONTROLLERS AND MICROCOMPUTER SYSTEMS

COURSE CODE: EE423

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.
2. If you think not enough data has been given in any question, you may assume any reasonable values stating your assumptions in each case.
3. You may find some useful data attached at the end of the paper.

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THIS PAPER CONTAINS SEVEN (6) PAGES INCLUDING THIS PAGE

QUESTION ONE *(25 marks)*

(a) (i) Describe the memory areas available and their use in a typical microcontroller.

(3 marks)

(ii) What is the architecture used in PIC16F84A device? State why this architecture is more faster.

(3 marks)

(iii) Identify the main features of RISC type microcontrollers.

(2 marks)

(iv) Differentiate between a typical microprocessor system and a microcontroller system.

(2 marks)

(b) A segment of a program using PIC16F84A is given in Figure-Q1.

```
option_reg   equ  01h
bsf          status,5
movlw        b'10000010'
movwf        option_reg
bcf          status,5
```

Figure-Q1

(i) Explain all the statements shown in Figure-Q1.

(5 marks)

(ii) It is required to have the timer TMR0 to overflow in each 10ms in a certain application. Crystal oscillators available are 1MHz, 2.0MHz, 2.457MHz, 3.277MHz and 3.579MHz. Recommend a suitable crystal justifying your answer and show the percentage timing error if any. Modify the assembly instructions in Figure-Q1 to accommodate your selection.

(8 marks)

(iii) Draw a circuit diagram to show how you will connect the crystal oscillator to the microcontroller.

(2 marks)

QUESTION TWO *(25 marks)*

(a) A 3 × 4 key pad shown in Figure-Q2(a) is required to be connected to PIC16F84A microcontroller using its PortB.

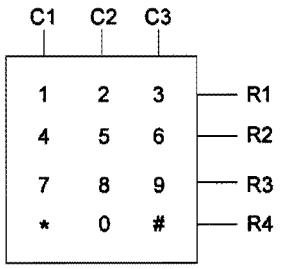


Figure-Q2(a)

```
delay   movlw   d8h
        movwf   delayreg
loop    nop
        nop
        decfsz  delayreg,1
        goto    loop
        return
```

Figure-Q2(b)

The keys '#' and '*' may have the decimal values of 10 and 11 respectively. A subroutine 'scan' finds the key pressed and store the binary value corresponding to the key in the register 'keycode'.

(i) Draw a diagram to show the interconnections between the keypad and the microcontroller. Indicate whether the port pins are inputs or outputs.

(3 marks)

(ii) Draw a labeled flow chart segment to show how a pressed key in column C1 is found and to store the value of the key in 'keycode'.

(5 marks)

(iii) Write the assembly code which will determine the scanning of key'1' and key'4' based on your flow chart in (ii) above. You may neglect the de-bounce effects.

(5 marks)

(b) A subroutine written to provide a delay is shown in Figure-Q2(b). It is a part of a program which runs in a 16F84A microcontroller clocked with a 8MHz crystal.

(i) Find the delay time produced by this subroutine.

(8 marks)

(ii) It is required to obtain a delay as close as $300\mu s$. Show how you can achieve it by changing only a single instruction. What is the percentage timing error?

(4 marks)

QUESTION THREE *(25 marks)*

A house heating system is designed based on a 16F84A microcontroller powered with 5V. A single boiler is used to heat the upstairs and downstairs, but are equipped with independently controlled flow pumps. Following system components are used and they accepts TTL compatible signals.

Signal	*Description*
T_B	Boiler water temperature sensor output. Returns logic '1' if the temperature is above the set limit.
T_U *and* T_D	Outputs of the upstairs and down stairs temperature sensors. Returns logic '0' if the temperature is less than the set value.
P_U *and* P_D	Control signals of the upstairs and downstairs flow pumps. Logic '1' applied to a control signal operates the pump.
H	Control signal of the boiler heater. Logic '1' applied to the control signal turns on the boiler heater.

(i) Draw a circuit diagram for this system showing all signal interconnections with the pin numbers of the microcontroller. You may omit the components required for the clock oscillator. Sensors and the controlled components can be shown as blocks.

(5 marks)

(ii) Suggest the control logic that you are going to implement by the microcontroller program.

(7 marks)

(iii) Draw a flowchart for the microcontroller program based on (ii) above.

(9 marks)

(iv) Using assembly instructions show how you are going to configure the ports as required.

(4 marks)

QUESTION FOUR (*25 marks*)

(a) A control system is implemented using a 16F84A microcontroller program.

(i) The value of INTCON register at the initialization is A8h. Explain what you can understand by this setup.

(2 marks)

(ii) While running the program, the INTCON register showed a value of 29h at some point. Interpret the information described by the INTCON register.

(2 marks)

(iii) When an interrupt occurs, state the events that will take place in the program counter, stack memory and GIE bit. Indicate the essential features to be included in an interrupt service routine.

(6 marks)

(iv) The program uses TMR0 timer to generate a regular interrupt in every 1ms. Show the settings needed in relevant registers to achieve this supported with relevant calculations. What is the value of INTCON register just after such an interrupt? Assume that the system uses a 2MHz crystal oscillator.

(6 marks)

(b) An application uses a PIC 16F877 microcontroller with a 10MHz crystal oscillator.

(i) It is required to use the Analog to Digital Converter (ADC) of the device with an external voltage reference and five analog input channels. Show the settings of the relevant registers with justification if the input channel 4 is selected and the ADC is turned on but not started to convert. You may assume that the ADC output is left justified.

(6 marks)

(ii) The ADC minimum acquisition time is about 20μs. State the relevance of this value and indicate how it is incorporated in a program.

(3 marks)

QUESTION FIVE (25 *marks*)

(a) A serial device which supports SPI is required to be connected to the Synchronous Serial Port of a PIC 16F877 microcontroller.

(i) Draw a circuit diagram to show the interconnections of the device and the microcontroller. You may consider the device pins such as DIN (data in), DOUT (data out), SCLK (serial clock) and $\overline{CS}$ (chip select). Mark only the relevant pin numbers of the microcontroller used for the interconnection.

(6 marks)

(ii) State briefly how the data is transferred between the device and the microcontroller using SPI mode.

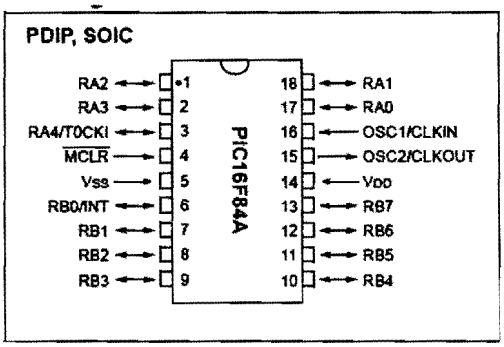
(9 marks)

(b) The serial device has a maximum data rate of 200kHz and the microcontroller is running on a 10MHz crystal oscillator.

Show the settings of the SSPCON, SSPSTAT and any other register involved to establish SPI mode of operation, giving justifications where necessary. Among other typical settings, you may include the settings for, the high idle state of clock, data sampling at the middle of the bit period and the data transfers are on the falling edge of the clock.

(10 marks)

PIC 16F84A



File Address			File Address
00h	Indirect addr.(1)	Indirect addr.(1)	80h
01h	TMR0	OPTION_REG	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	—	—	87h
08h	EEDATA	EECON1	88h
09h	EEADR	EECON2(1)	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	68 General Purpose Registers (SRAM)	Mapped (accesses) in Bank 0	8Ch
4Fh			CFh
50h			D0h

STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Unimplemented: Maintain as '0'

RP0: Register Bank Select bits (used for direct addressing)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

$\overline{TO}$: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

$\overline{PD}$: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

DC: Digit carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

C: Carry/$\overline{borrow}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

SMP: Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in slave mode
In I^2C Master or Slave mode:
1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for high speed mode (400 kHz)

CKE: SPI Clock Edge Select (Figure 9-2, Figure 9-3 and Figure 9-4)
SPI mode:
For CKP = 0
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK
For CKP = 1
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK
In I^2C Master or Slave mode:
1 = Input levels conform to SMBus spec
0 = Input levels conform to I^2C specs

D/A: Data/$\overline{\text{Address}}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

P: STOP bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
0 = STOP bit was not detected last

S: START bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
0 = START bit was not detected last

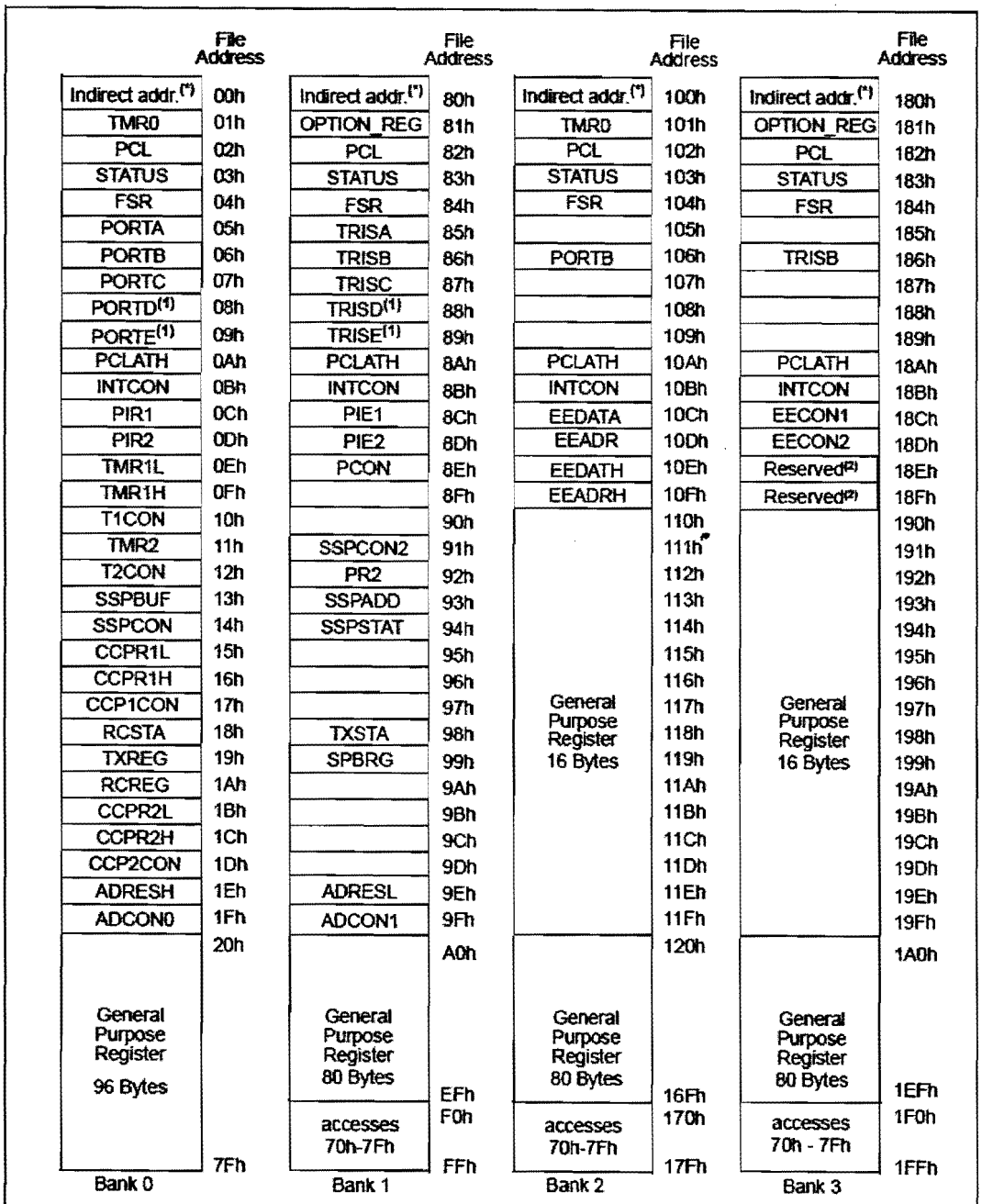
R/W: Read/Write bit Information (I^2C mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit or not $\overline{\text{ACK}}$ bit.
In I^2C Slave mode:
1 = Read
0 = Write
In I^2C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
Logical OR of this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.

UA: Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

BF: Buffer Full Status bit
Receive (SPI and I^2C modes):
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit (I^2C mode only):
1 = Data transmit in progress (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is full
0 = Data transmit complete (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is empty

PIC 16F877

PIC16F877/876 REGISTER FILE MAP



Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876.

2: These registers are reserved, maintain these registers clear.

ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

ADFM: A/D Result Format Select bit
1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

Unimplemented: Read as '0'

PCFG3:PCFG0: A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7[1] RE2	AN6[1] RE1	AN5[1] RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs[2]
0000	A	A	A	A	A	A	A	A	VDD	Vss	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	Vss	7/1
0010	D	D	D	A	A	A	A	A	VDD	Vss	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	Vss	4/1
0100	D	D	D	D	A	D	A	A	VDD	Vss	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	Vss	2/1
011x	D	D	D	D	D	D	D	D	VDD	Vss	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	Vss	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	Vss	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	Vss	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input D = Digital I/O

Note 1: These channels are not available on PIC16F873/876 devices.
2: This column indicates the number of analog channels available as A/D inputs and the number of analog channels used as voltage reference inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown