UNIVERSITY OF ESWATINI

MAIN EXAMINATION, SECOND SEMESTER MAY 2019

FACULTY OF SCIENCE AND ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

TITLE OF PAPER: INTRODUCTION TO PROGRAMMABLE ARRAYS AND
MICROCONTROLLERS

COURSE CODE: EEE324

TIME ALLOWED: THREE HOURS

INSTRUCTIONS:

1. There are five questions in this paper. Answer any FOUR questions. Each question carries 25 marks.

2. If you think not enough data has been given in any question, you may assume any reasonable values stating your assumptions in each case.

3. You may find some useful data at the end of the paper.

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THIS PAPER CONTAINS SIX (6) PAGES INCLUDING THIS PAGE

QUESTION ONE (25 marks)

(a)   What is meant by $2K \times 8$ ROM? State the number of address lines required in this ROM.

(3 marks)

(b)   Implement a static RAM of $6K \times 8$ using $2K \times 8$ RAM integrated circuits.

The available $2K \times 8$ RAM ICs have independent Data Inputs, 3-state Data Outputs, Address, Enable and $R/\bar{W}$ lines. You need to show clearly the connection of these lines in your design with necessary information.

(7 marks)

(c)   (i) Briefly differentiate the types of programmable logic devices used for combinational logic implementations.

(5 marks)

(ii) Using a single PLA, implement the following logic functions.

$A(a,b,c) = \Sigma (0,2,5,7)$

$B(a,b,c) = \Sigma (1,3,4,7)$

Your design must have a minimum number of product terms. Provide the programming table and draw the connection map. Specify the minimum size of the PLA required.

(10 marks)

QUESTION TWO *(25 marks)*

(a)   Describe briefly the Von-Neumann's and Harvard architectures.

(4 marks)

(b)   Using a block diagram, show the hardware organization of a microprocessor based system for the requirements given below and identifying the use of each block.

The requirements are, 20 digital I/O lines, 3 external H/W interrupt lines, 5 analog input lines, 5 analog output lines and serial communication facilities.

(6 marks)

(c)   State the use of SFRs and GPRs with respect to 16F84A device.

(4 marks)

(d)   Explain the events using your own words that will occur when executing the instruction *'retlw .25'* in 16F84A.

(5 marks)

(e)   Write the machine codes (op-codes) of 16F84A for the following instructions.
   movlw .53
   btfss portA, 2
   decf portB, w

(6 marks)

QUESTION THREE *(25 marks)*

The $PortB(7)$ of a 16F84A drives a LED by a push button switch (active low) connected to $PortA(0)$.

When the push button switch is pressed, the LED should be *ON* for 1.5 seconds and then *OFF*. Once the switch is pressed, it should be non-responsive for a period of 3 seconds before it is responsive again. This process should continue repeatedly.

Assume that the 16F84A is used with a $40kHz$, RC clock.

(a)   Draw the complete hardware circuit for this application showing the pin numbers of 16F84A. State the functions of the external components connected. No need to provide any component values.

(6 marks)

(b)   Draw a flow chart/s for this problem which can be a sufficient aid to write a program. You may neglect the effects of the switch bounce.

(10 marks)

(c)   Write the assembly code for the following sections of a program based on your flow chart stating any assumptions and derivation of values used.

- Configuration of ports and other important registers.

(3 marks)

- Producing the delay of 1.5 seconds.

(6 marks)

QUESTION FOUR *(25 marks)*

(a) You may assume 16F84A microcontroller for the following.

    (i)   State the interrupt sources of this device.

            (4 marks)

    (ii)   When running a program, the value of INTCON is $32h$ at a certain instant. Explain what is shown by this value. Write the settings of the INTCON at initialization.

            (4 marks)

    (iii)   In a program, pre scaling is set to 32. Find the longest period of a regular interrupt that can be possible to generate with a $10MHz$ crystal oscillator.
Show the initial settings needed in the relevant registers under this circumstances.

            (7 marks)

(b) Following is to be used with a PIC 16F877 microcontroller using a $10MHz$ crystal oscillator.

    (i)   If the Analog to Digital Converter (ADC) of the device is to be used, show the settings of the relevant registers for the following.

        •   Three analog inputs with $RE(0)$ as a digital output line.

        •   An external $+ve$ voltage reference with $-ve$ reference voltage equals zero.

        •   Analog channel 0 is selected and the ADC is turned on but not started to convert.

        •   The ADC output is left justified.

            (6 marks)

    (ii)   It is said that an 'acquisition time' should be observed in connection with a ADC. State with your own words, the relevance of this and how it is usually used in a program for 16F877.

            (4 marks)

QUESTION FIVE (25 *marks*)

(a)   A device with UART interface having a baud rate of $28KB/s$ is to be connected to a 16F877 microcontroller. The connection is full duplex and asynchronous. A crystal oscillator of $16MHz$ is used and 8 bit data transfer is assumed.

     (i)   Draw a clear interconnection diagram between the devices. Clearly mark the relevant pin numbers and pin names of 16F877 used.

                           (2 marks)

     (ii)   Show the settings of the registers TXSTA, SPBRG and RCSTA assuming high speed selection. What is the percentage error in the baud rate?

                           (9 marks)

     (iii)   State briefly how the data is exchanged between the devices.

                           (4 marks)

(b)   A device having SPI is expected to communicate using a data rate of $150Kb/s$ with a 16F877 microcontroller. The microcontroller clock is $8MHz$.

     (i)   Draw an interconnection diagram marking the relevant. pin names and pin numbers of 16F877 and the device. You may use standard pin names for the device. Mark **only** the pins used for the interconnection.

                           (2 marks)

     (ii)   Show the settings of the SSPCON and SSPSTAT for the timing waveforms of the device shown in Figure-Q5.
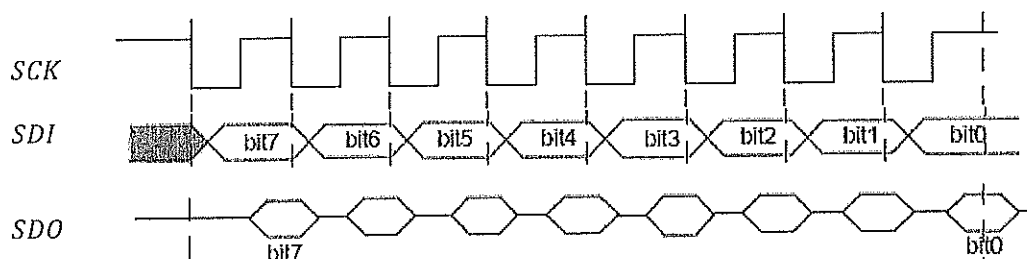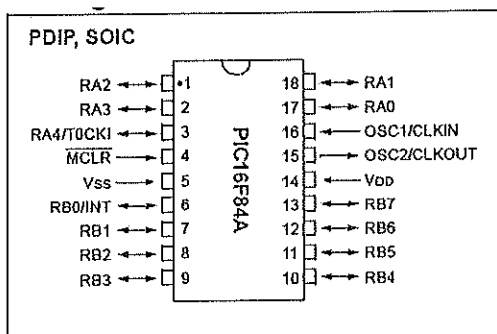

Figure-Q5

                           (8 marks)

PIC 16F84A

PDIP, SOIC

```
            ┌───┬───┐
RA2  ◄──► □ •1      18 □ ◄──► RA1
RA3  ◄──► □  2      17 □ ◄──► RA0
RA4/T0CKI ◄──► □ 3  16 □ ◄── OSC1/CLKIN
MCLR ──► □  4   P   15 □ ──► OSC2/CLKOUT
Vss  ──► □  5   I   14 □ ◄── VDD
RB0/INT ◄──► □ 6 C  13 □ ◄──► RB7
            1
RB1  ◄──► □  7   6  12 □ ◄──► RB6
            F
RB2  ◄──► □  8   8  11 □ ◄──► RB5
            4
RB3  ◄──► □  9   A  10 □ ◄──► RB4
            └───────┘
```

File Address			File Address
00h	Indirect addr.[1]	Indirect addr.[1]	80h
01h	TMR0	OPTION_REG	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h	EEDATA	EECON1	88h
09h	EEADR	EECON2[1]	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch			8Ch
	68 General Purpose Registers (SRAM)	Mapped (accesses) in Bank 0	
4Fh			CFh
50h			D0h

STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

bit 7   bit 0

Unimplemented: Maintain as '0'

RP0: Register Bank Select bits (used for direct addressing)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

$\overline{TO}$: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

$\overline{PD}$: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for borrow, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for borrow, the polarity is reversed)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

PIC 16F84A

OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

bit 7   bit 0

RBPU: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

INTEDG: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

T0CS: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

T0SE: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

PSA: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF

bit 7   bit 0

GIE: Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

EEIE: EE Write Complete Interrupt Enable bit
1 = Enables the EE Write Complete interrupts
0 = Disables the EE Write Complete interrupt

T0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

INTE: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

RBIE: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

T0IF: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

INTF: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

RBIF: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
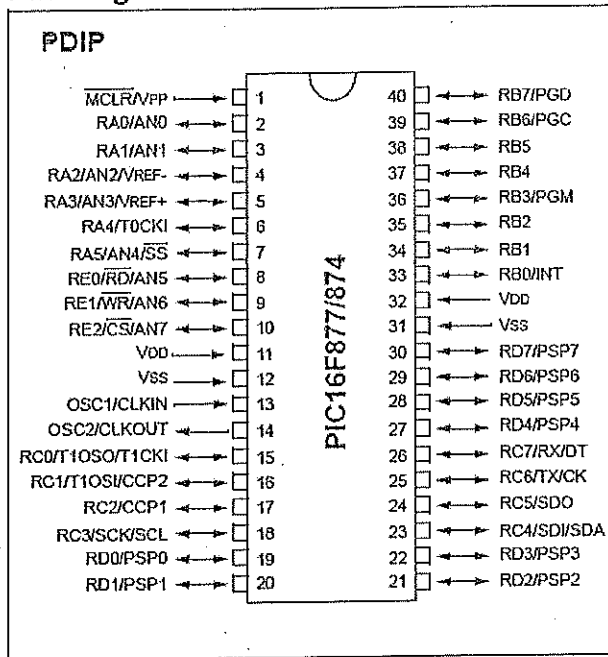0 = None of the RB7:RB4 pins have changed state

16F84A and 16F877

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from Interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

PIC 16F877

Pin Diagram

PDIP

MCLR/Vpp →	1	40 ← → RB7/PGD
RA0/AN0 ← →	2	39 ← → RB6/PGC
RA1/AN1 ← →	3	38 ← → RB5
RA2/AN2/VREF- ← →	4	37 ← → RB4
RA3/AN3/VREF+ ← →	5	36 ← → RB3/PGM
RA4/T0CKI ← →	6	35 ← → RB2
RA5/AN4/SS ← →	7	34 ← → RB1
RE0/RD/AN5 ← →	8	33 ← → RB0/INT
RE1/WR/AN6 ← →	9	32 ← VDD
RE2/CS/AN7 ← →	10	31 ← Vss
VDD →	11	30 ← → RD7/PSP7
VSS →	12	29 ← → RD6/PSP6
OSC1/CLKIN →	13	28 ← → RD5/PSP5
OSC2/CLKOUT ←	14	27 ← → RD4/PSP4
RC0/T1OSO/T1CKI ← →	15	26 ← → RC7/RX/DT
RC1/T1OSI/CCP2 ← →	16	25 ← → RC6/TX/CK
RC2/CCP1 ← →	17	24 ← → RC5/SDO
RC3/SCK/SCL ← →	18	23 ← → RC4/SDI/SDA
RD0/PSP0 ← →	19	22 ← → RD3/PSP3
RD1/PSP1 ← →	20	21 ← → RD2/PSP2

PIC16F877/874

SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

bit 7   bit 0

SMP: Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in slave mode
In I^2C Master or Slave mode:
1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for high speed mode (400 kHz)

CKE: SPI Clock Edge Select (Figure 9-2, Figure 9-3 and Figure 9-4)
SPI mode:
For CKP = 0
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK
For CKP = 1
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK
In I^2C Master or Slave mode:
1 = Input levels conform to SMBus spec
0 = Input levels conform to I^2C specs

D/A: Data/Address bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

P: STOP bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
0 = STOP bit was not detected last

S: START bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
0 = START bit was not detected last

R/W: Read/Write bit Information (I^2C mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit or not ACK bit.
In I^2C Slave mode:
1 = Read
0 = Write
In I^2C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
Logical OR of this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.

UA: Update Address (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

BF: Buffer Full Status bit
Receive (SPI and I^2C modes):
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty
Transmit (I^2C mode only):
1 = Data transmit in progress (does not include the ACK and STOP bits), SSPBUF is full
0 = Data transmit complete (does not include the ACK and STOP bits), SSPBUF is empty

SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0

bit 7   bit 0

WCOL: Write Collision Detect bit

Master mode:
1 = A write to SSPBUF was attempted while the I2C conditions were not valid
0 = No collision

Slave mode:
1 = SSPBUF register is written while still transmitting the previous word (must be cleared in software)
0 = No collision

SSPOV: Receive Overflow Indicator bit

In SPI mode:
1 = A new byte is received while SSPBUF holds previous data. Data in SSPSR is lost on overflow. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid overflows. In Master mode, the overflow bit is not set, since each operation is initiated by writing to the SSPBUF register. (Must be cleared in software.)
0 = No overflow

In I^2C mode:
1 = A byte is received while the SSPBUF is holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software.)
0 = No overflow

SSPEN: Synchronous Serial Port Enable bit

In SPI mode,
When enabled, these pins must be properly configured as input or output
1 = Enables serial port and configures SCK, SDO, SDI, and SS as the source of the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

In I^2C mode,
When enabled, these pins must be properly configured as input or output
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

CKP: Clock Polarity Select bit

In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level

In I^2C Slave mode:
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

In I^2C Master mode:
Unused in this mode

SSPM3:SSPM0: Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = Fosc/4
0001 = SPI Master mode, clock = Fosc/16
0010 = SPI Master mode, clock = Fosc/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin. SS pin control enabled.
0101 = SPI Slave mode, clock = SCK pin. SS pin control disabled. SS can be used as I/O pin.
0110 = I^2C Slave mode, 7-bit address
0111 = I^2C Slave mode, 10-bit address
1000 = I^2C Master mode, clock = Fosc / (4 * (SSPADD+1))
1011 = I^2C Firmware Controlled Master mode (slave idle)
1110 = I^2C Firmware Controlled Master mode, 7-bit address with START and STOP bit interrupts enabled
1111 = I^2C Firmware Controlled Master mode, 10-bit address with START and STOP bit interrupts enabled
1001, 1010, 1100, 1101 = Reserved

PIC 16F877

PIC16F877/876 REGISTER FILE MAP

File Address		File Address		File Address		File Address	
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h		108h		188h
PORTE(1)	09h	TRISE(1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h		110h		190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h	General Purpose Register 16 Bytes	117h	General Purpose Register 16 Bytes	197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch		9Ch		11Ch		19Ch
CCP2CON	1Dh		9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	
			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h - 7Fh	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

▓ Unimplemented data memory locations, read as '0'.
* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876.
2: These registers are reserved, maintain these registers clear.

ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE		ADON

bit 7 — bit 0

ADCS1:ADCS0: A/D Conversion Clock Select bits
00 = Fosc/2
01 = Fosc/8
10 = Fosc/32
11 = FRC (clock derived from the internal A/D module RC oscillator)

CHS2:CHS0: Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)[1]
110 = channel 6, (RE1/AN6)[1]
111 = channel 7, (RE2/AN7)[1]

GO/DONE: A/D Conversion Status bit
If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

Unimplemented: Read as '0'

ADON: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shut-off and consumes no operating current

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ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0

bit 7   bit 0

ADFM: A/D Result Format Select bit
1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

Unimplemented: Read as '0'

PCFG3:PCFG0: A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7[1] RE2	AN6[1] RE1	AN5[1] RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs[2]
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input   D = Digital I/O

Note 1: These channels are not available on PIC16F873/876 devices.
    2: This column indicates the number of analog channels available as A/D inputs and the number of analog channels used as voltage reference inputs.

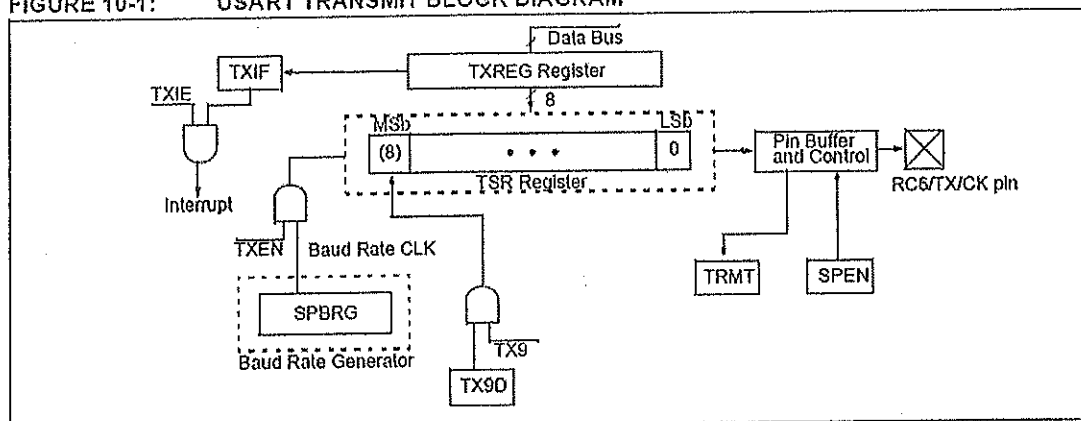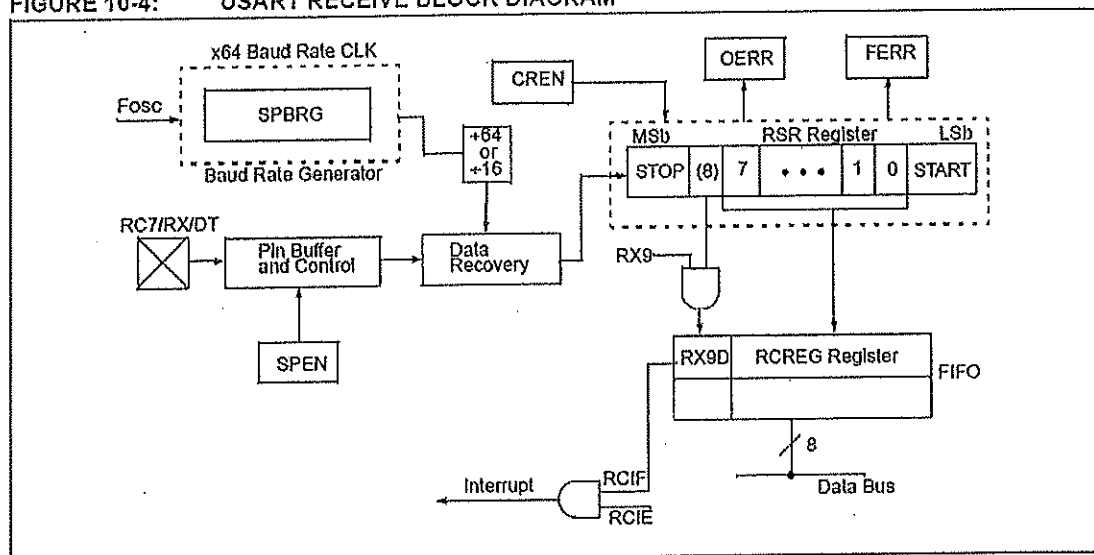| Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

FIGURE 10-1:   USART TRANSMIT BLOCK DIAGRAM

FIGURE 10-4:   USART RECEIVE BLOCK DIAGRAM

TXSTA:	CSRC	TX9	TXEN	SYNC	-	BRGH	TRMT	TX9D

RCSTA:	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RXPD

$$BR_H = \frac{F_{osc}}{16(X+1)} \qquad BR_L = \frac{F_{osc}}{64(X+1)}$$

SPI Mode Waveform (Master Mode)